Initial (bad) scan chain order

Optimized scan chain order

Figure 1

Pattern		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Latch 200	Input	0	1	0	0	0	1	1	0	1	1	0	1	0	1	0	1	same
	Result	1	1	1	0	1	1	0	0	1	0	0	1	1	0	0	0	
Latch 210	Input	0	1	0	0	0	1	1	0	1	1	0	1	0	1	0	1	opposite
	Result	0	0	0	1	0	0	1	1	0	1	1	0	0	1	1	1	
Latch 220	Input	0	1	0	0	0	1	1	0	1	1	0	1	0	1	0	1	same
	Result	1	1	1	0	1	1	0	0	1	0	0	1	1	0	0	0	

Figure 2

Logic

Latches

	1
	2
	3
	4
	5
	6
	7
	8
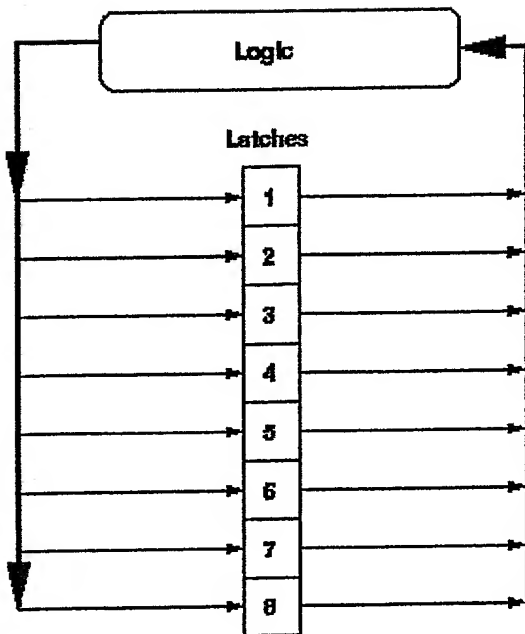
Initial values		Pass 1		Pass 2		Pass 2	
Input	Result	Input	Result	Input	Result	Input	Result
1	X	1	(1)	1	1	1	1
0	1	0	1	0	1	0	1
X	0	X	0	(1)	0	1	0
X	0	X	0	X	0	(0)	0
X	X	X	(0)	(0)	0	0	0
1	X	1	X	1	(1)	1	1
X	1	(1)	1	1	1	1	1
X	1	X	1	(0)	1	0	1

Set input 7   Set result 6   Set result 4

Values in solid circles are set, values in dashed
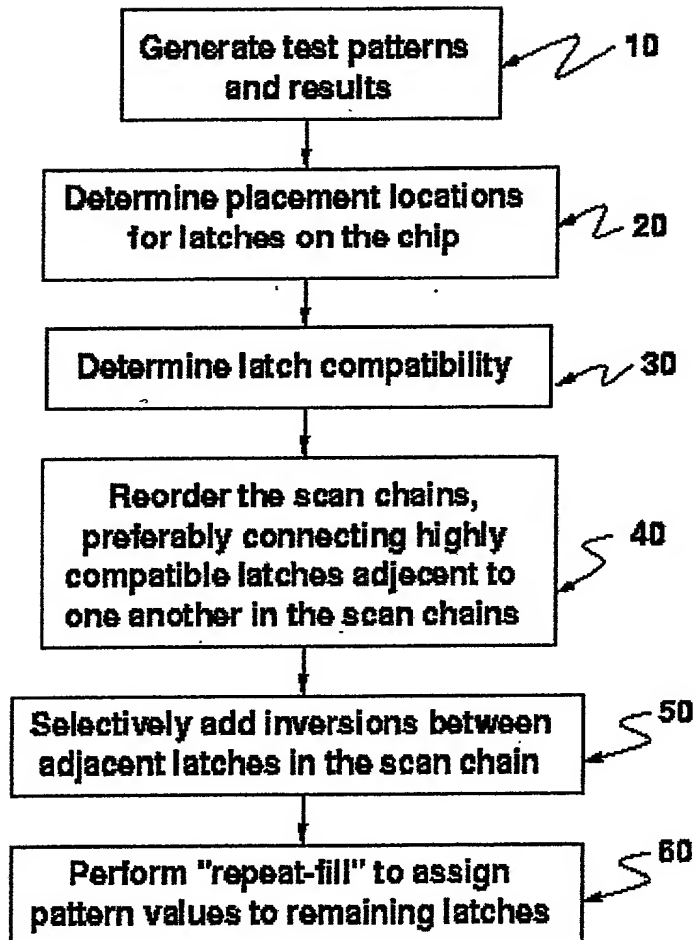circles are implied by these settings

Figure 3

Generate test patterns
and results
⟋ 10

Determine placement locations
for latches on the chip
⟋ 20

Determine latch compatibility
⟋ 30

Reorder the scan chains,
preferably connecting highly
compatible latches adjacent to
one another in the scan chains
⟋ 40

Selectively add inversions between
adjacent latches in the scan chain
⟋ 50

Perform "repeat-fill" to assign
pattern values to remaining latches
⟋ 60

Figure 4